REMARKS

In response to the Official Action mailed January 16, 2003, Applicant amends his application and requests reconsideration. In this Amendment, claims 9-12 are cancelled and claims 13-16 are added so that claims 1-8 and 13-16 are now pending.

The Examiner objected to the specification erroneously referring to 35 U.S.C. 112, first paragraph. That statutory section pertains to the claims and whether claims are supported by the disclosure of a patent application, not to potential difficulty in understanding a specification. In response to the Examiner's comments, appropriate changes have been made to the paragraphs including the two items cited. A review has been made of the specification. While the specification may not be in the highest quality English, the specification is readily understood by one of skill in the relevant art. In view of the burden of rewriting the specification, Applicant submits that the specification meets the minimum standard required by the U.S. Patent and Trademark Office.

Claims 7 and 8 were stated to be allowable. Those claims remain pending as dependent claims, depending from claim 5. No further comment on those claims is necessary. Claims 14 and 15 have the same limitations as claims 7 and 8 and are therefore allowable.

Of the remaining examined claims, claims 1-6 were rejected as unpatentable over Ma et al. (U.S. Patent 5,939,753, hereinafter Ma) in view of Wang (U.S. Patent 6,351,363). This rejection is respectfully traversed.

Claims 1, 2, and 3 are clearly supported in the patent application, for example by Figure 10 and the description pertaining to that figure.

Claims 1 and 2 have been amended so that both claims are independent claims. The claims are analogous claims. In the structure of amended claim 1, m lateral polysilicon diodes are connected in series and in the forward direction between a high frequency I/O signal line to an externally supplied voltage, VDD. In the semiconductor device structure of claim 2, n lateral polysilicon diodes are connected in series in the forward direction between ground and the high frequency I/O signal line. There are at least two diodes in each arrangement since m and n are both positive integers greater than 1. In both structures, the maximum reverse bias voltage applied to the lateral polysilicon diodes is smaller than 1.1 volts. This voltage, roughly equal to the band gap "voltage" of silicon, ensures that the diodes do not break down.

The structure in claim 3 combines the elements of claims 1 and 2 with some exceptions. In the structures defined by claims 1 and 2, m or n is at least 2. In the structure of claim 3, m or n can be 1, although both m and n cannot be 1.

The most pertinent part of the disclosures of Wang and Ma appears in Figures 3 and 4 of Wang. Those figures show arrangements of two diodes connected in series between a ground line and a high voltage line that supply power to an internal circuit. Multiple pairs of such diodes are provided and the diodes are resistively interconnected at the respective nodes of the pairs of diodes. Further, those nodes are connected to the input terminal of the circuits illustrated in Figures 3 and 4 of Wang. Thus, there is, at most, one diode connected between the high voltage line and an input/output line and one diode connected between the input/output node and the ground line. Therefore, Wang fails to disclose the arrangement described in either of claims 1 and 2 including multiple lateral polysilicon diodes connected between the high voltage line and the high frequency I/O signal line or multiple lateral polysilicon diodes connected between the high frequency I/O signal line and ground. Ma adds nothing pertinent to the relevant disclosure of Wang that might suggest the invention as defined by claims 1 and 2. Therefore, the rejection should be withdrawn.

Claim 3 describes a high-frequency semiconductor device including a plurality of lateral polysilicon diodes connected in series between an I/O signal line and a high voltage power source and another series connection of lateral polysilicon diodes connected between the signal line and ground. This arrangement is not illustrated or suggested in either of Ma or Wang. As already noted, Wang shows, in Figures 3 and 4, structures in which polysilicon diodes are connected in series in pairs between a high voltage line and ground. Each node between each pair of diodes connected to an input line. It is apparent that what is disclosed in Wang is the connection of diodes between an I/O line and the high voltage line in parallel, not in series.

The arrangement illustrated in Wang does not suggest the series connection of lateral polysilicon diodes as in the invention. In the parallel-connected arrangement of Wang, the breakdown voltage between the nodes where the diodes are commonly connected and the high voltage power line is the voltage of a single diode. In the structure described in claim 3, the breakdown voltage depends upon the number of diodes connected in series. This very different concept is not suggested by Wang. Therefore, Ma as modified by Wang cannot disclose all of the limitations of claim 3 and cannot establish *prima facie* obviousness of that claim or its dependent claim 4.

Claims 5 and 6 describe an ESD protection structure including not only polysilicon diodes but also a capacitor. In the structure described in claim 5, there are two such polysilicon electrodes for the capacitor and the polysilicon layer used to form one of those electrodes is also part of the first lateral polysilicon diode. A second polysilicon layer is used to form the gate of the MOS transistor. In the structure described in claim 6, the polysilicon gate of the MOS

transistor is made from the same polysilicon film that is employed as the upper electrode of the capacitor.

Claims 5 and 6 were rejected commonly, with the assertion that Ma discloses a transistor with polysilicon upper and lower electrodes and a transistor having a polysilicon gate. Even assuming that assertion is correct, the Examiner has not explained how the teaching of Wang would produce the structures described in claims 5 and 6. Applicant agrees that Wang apparently teaches a polysilicon diode, using the odd term "polydiode". However, there is no description of any capacitor within Wang and therefore there can be no suggestion of any sharing of capacitor plates and transistor gates in common polysilicon layers. In other words, Wang cannot suggest the modification of Ma that would be necessary as a basis for a proper rejection of claims 5 and 6 as obvious. Therefore, upon reconsideration, the rejection of those claims should be withdrawn.

Reconsideration and allowance of all pending claims, claims 3-8 and 13-16, are appropriate and earnestly solicited.

Respectfully submitted,

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